What is claimed is:

1. A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage.

2. A clock multiplication circuit according to claim 1,

wherein the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is at either a High level or a Low level,

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the count value is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the counting period and before the start of a succeeding counting period.

3. A clock multiplication circuit according to claim 1, wherein the counter is counter for obtaining the count value at end of every High level period and every Low level period.

4. A clock multiplication circuit according to claim 1, wherein:

the counter is a counter for obtaining the count value at end of every High level period and every Low level period,

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics in which when the count value obtained by counting during a certain High level period is changed from a preceding count value, the frequency of the output clock signal is changed from the end of the High level period to the start of next High level period; and

the characteristics in which when the count value obtained by counting during a certain Low level period is changed from a preceding count value, the frequency of the output clock signal is changed after end of the Low level period and before the start of the succeeding Low level period.

5. A clock multiplication circuit according to claim 1, wherein the counter delivers the count value after the end of the counting period and in synchronization with the output clock signal, the subtracter delivers the difference value after the end of the counting period and in synchronization with the output clock signal, and the control voltage generation circuit delivers the analog control voltage after the end of the counting period and in synchronization with the output clock signal.

6. A clock multiplication circuit according to claim 1, wherein

both rising edges and falling edges of the output clock signal are taken as the effective transition edges by the counter.

7. A clock multiplication circuit according to claim 1, wherein a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage generation circuit is interposed between the subtracter and the control voltage generation circuit.

8. A clock multiplication circuit according to claim 7, wherein the multiplier comprised of a shift register for implementing bit shift of the difference value by predetermined bits.

9. A clock multiplication circuit according to claim 7, wherein a factor of the multiplier is variable.

10. A clock multiplication circuit according to claim 9, further comprising factor control means for controlling the factor of the multiplier, the factor control means being capable of raising the factor to a relatively high number during a lock-in period, and lowering the factor to a relatively low number after the end of the lock-in period.

11. A clock multiplication circuit according to claim 1, wherein the subtracter is capable of switching the reference value.

12. A clock multiplication circuit according to claim 11, wherein the subtracter comprises reference value storage means for storing the reference value, the reference value storage means

configured so as to enable the reference value to be stored in the reference value storage means from outside.

13. A clock multiplication circuit according to claim 1,

wherein the control voltage generation circuit comprises an adder for obtaining a new integrated value by adding the difference value to an integrated value obtained in a preceding counting period and a DA converter circuit for converting the new integrated value into the analog control voltage.

14. A clock multiplication circuit according to claim 13, further comprising initial integrated value acquisition means for acquiring an initial integrated value to be used by the adder after the clock multiplication circuit is powered on or is reset.

15. A clock multiplication circuit according to claim 14,

wherein the initial integrated value acquisition means comprises:

quasi-integrated value generation means for inputting a quasi-integrated value instead of the integrated value from the adder to the DA converter circuit, sequentially varying the quasi-integrated value; and

quasi-value storage means for storing the quasi-integrated value and a quasi-count value obtained by counting the number of the effective transition edges of the output clock signal delivered on the basis of the quasi-integrated value during the counting period so as to correspond to each other against each of the quasi-integrated values,

the initial integrated value acquisition means taking a quasi-integrated value corresponding to a quasi-count value equal

to, or closest to the reference value as an initial integrated value.

16. A clock multiplication circuit according to claim 14, wherein the initial integrated value acquisition means comprises:

quasi-integrated value generation means for inputting a quasi-integrated value instead of the integrated value from the adder to the DA converter circuit; and

determination means for determining whether or not a quasi-difference value as calculated by use of the reference value and a quasi-count value obtained by counting the number of the effective transition edges of the output clock signal delivered on the basis of the quasi-integrated value during the counting period is within a predetermined numerical value range including 0, taking the present quasi-difference value as the initial integrated value when the quasi-difference value is within the predetermined numerical value range, and causing the quasi-integrated value generation means to vary the quasi-integrated value such that a successively calculated quasi-difference value becomes closer to 0 than the present quasi-difference value to input to the DA converter circuit when the present quasi-difference value is not within the predetermined numerical value range.

17. A clock multiplication circuit according to claim 13,

wherein the initial integrated value acquisition means is a nonvolatile memory that sequentially overwrites and stores the integrated value obtained by the adder.

18. A clock multiplication circuit according to claim 14,

wherein the initial integrated value acquisition means is preceding integrated value storage means for storing a present

integrated value, as calculated by the adder, in a nonvolatile memory at the time when the clock multiplication circuit is powered off.

19. A clock multiplication circuit according to claim 14,

wherein the initial integrated value acquisition means is preceding integrated value storage means for storing the integrated value that was used when the output clock signal at the frequency that is the multiple of the frequency of the reference clock signal was being outputted the last time the clock multiplication circuit was in use.

20. A clock multiplication circuit according to claim 1,

wherein the analog control voltage generation circuit comprises a DA converter for converts the difference value into an analog difference voltage, and

an analog integration circuit for integrating the analog difference voltage to thereby obtain the analog control voltage.

21. A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

an oscillation circuit for delivering the output clock signal; and

an oscillation control circuit for controlling the frequency of the output clock signal from the oscillation circuit such that

the count value becomes equal to a predetermined reference value.

22. A clock multiplication circuit according to claim 21, further comprising integration means for integrating the count value either digitally or analogically.